



Static Timing Analysis for Nanometer Designs

A Practical Approach

J. Bhasker
Rakesh Chadha



Springer

Static Timing Analysis For Nanometer Designs A Practical Approach

Jiajia Wang

Static Timing Analysis For Nanometer Designs A Practical Approach:

Static Timing Analysis for Nanometer Designs J. Bhasker, Rakesh Chadha, 2009-04-03
Timing is the main concern of a digital designer charged with designing a semiconductor chip. What is timing? How is it described and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, timing closure is the major milestone which dictates when a chip can be leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently available that can be used by a working engineer to get acquainted with the details of static timing analysis. The chip designers lack a central reference for information on timing that covers the basics to the advanced timing verification procedures and techniques.

A Practical Approach to VLSI System on Chip (SoC) Design Veena S. Chakravarthi, 2019-09-25

This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system-on-chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low-power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade and will also be a valuable professional reference for those already working in VLSI design and verification, with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers, it covers end-to-end VLSI SoC design flow, including source code, case studies, and application examples.

Constraining Designs for Synthesis and Timing Analysis Sridhar Gangadharan, Sanjay Churiwala, 2014-07-08
This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis, and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

Introduction to VLSI Design Flow Sneh Saurabh, 2023-06-15
Chip designing is a complex task that requires an in-depth understanding of VLSI design flow skills to employ sophisticated design tools and keep pace with the bleeding-edge semiconductor technologies. This lucid textbook is focused on fulfilling these requirements for students as well as a refresher for professionals in the industry. It helps the user develop a holistic view of the design flow through a well-sequenced set of chapters on logic synthesis, verification, physical design, and testing. Illustrations and pictorial representations have been used liberally to

simplify the explanation Additionally each chapter has a set of activities that can be performed using freely available tools and provide hands on experience with the design tools Review questions and problems are given at the end of each chapter to revise the concepts Recent trends and references are listed at the end of each chapter for further reading

Recent Advances and Emerging Challenges in STEM Yadir Torres,Ana M. Beltran,Manuel Felix,Estela Peralta,Diego F. Larios,2024-08-11 This book covers the works presented at the workshop aimed at bridging academia industry and society

fostering collaboration among lecturers technicians researchers and students It delves into functional materials tribo mechanical behavior bio residues and biopolymers Some chapters explore computer architecture artificial intelligence smart cities sustainable industries and life cycle assessment Additionally the book addresses emerging pollutants cellular and bacterial behavior powder technology applied physics applied mathematics industrial and environmental chemistry product design industrial robotic systems and deep learning systems

The British National Bibliography Arthur James

Wells,2009 **Integrated Circuit and System Design** ,2005 Proceedings ,2004 **Dissertation Abstracts**

International ,2008 *Novel Static Timing Analysis Approach for Customized Design Fabric* Jiajia Wang,2018 Synopsys PrimeTime is widely used for static timing analysis and timing signoff solutions nowadays However PrimeTime has its two limitation Firstly it is unable to work on some customized fabric where the circuit consist not only the standard cells and wires as in conventional circuit Secondly PrimeTime reports the timing of the design not as accurate in deep nanotechnology The error could sometimes be as large as 15% compare to the real case In this article we proposed a novel STA approach that combines the HSpice simulation and PrimeTime analysis to provide timing accuracy that is comparable to HSpice This approach is very flexible that could work on any non standard customized circuit including SRAM cell or customized circuit that containing pass transistors The thesis also introduced a customized design circuit named Field Programmable Transistor Array FPTA as test case to practically proved the feasibility of the new STA approach The simulation result shows that the proposed approach could work on nonstandard circuit and provide the accuracy that is extremely close to Spice simulation

The Art of Timing Closure Khosrow Golshan,2020-08-03 The Art of Timing Closure is written using a hands on approach to describe advanced concepts and techniques using Multi Mode Multi Corner MMMC for an advanced ASIC design implementation It focuses on the physical design Static Timing Analysis STA formal and physical verification The scripts in this book are based on Cadence Encounter SystemTM However if the reader uses a different EDA tool that tool s commands are similar to those shown in this book The topics covered are as follows Data Structures Multi Mode Multi Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth the author emphasizes short clear descriptions which are implemented by references to authoritative manuscripts It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design and to show the reader that physical design and timing analysis engineering

should be viewed as a single area of expertise This book is intended for anyone who is involved in ASIC design implementation starting from physical design to final design signoff Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design **Science Abstracts** ,1995

The Engineering Index Annual ,1992 Since its creation in 1884 Engineering Index has covered virtually every major engineering innovation from around the world It serves as the historical record of virtually every major engineering innovation of the 20th century Recent content is a vital resource for current awareness new production information technological forecasting and competitive intelligence The world s most comprehensive interdisciplinary engineering database Engineering Index contains over 10 7 million records Each year over 500 000 new abstracts are added from over 5 000 scholarly journals trade magazines and conference proceedings Coverage spans over 175 engineering disciplines from over 80 countries Updated weekly

Refactoring-based Statistical Timing Analysis and Its Applications to Robust Design and Test Synthesis Jae Yong Chung,2011 Technology scaling in the nanometer era comes with a significant amount of process variation leading to lower yield and new types of defective parts These challenges necessitate robust design to ensure adequate yield and smarter testing to screen out bad chips Statistical static timing analysis SSTA enables this but suffers from crude approximation algorithms This dissertation first studies the underlying theories of timing graphs and proposes two fundamental techniques enhancing the core statistical timing algorithms We first propose the refactoring technique to capture topological correlation Static timing analysis is based on leveled breadth first traversal which is a fundamental graph traversal technique and has been used for static timing analysis over the past decades We show that there are numerous alternatives to the traversal because of an algebraic property the distributivity of addition over maximum This new interpretation extends the degrees of freedom of static timing analysis which is exploited to improve the accuracy of SSTA We also propose a novel operator for computing joint probabilities in SSTA In many SSTA applications this is very common but is done using the max operator which results in much error due to the linear approximation The new operator provides significantly higher accuracy at a small cost of run time Second based on the two fundamental studies this dissertation devel ops three applications We propose a criticality computation method that is essential to robust design and test synthesis The proposed method combined with the two fundamental techniques achieves drastic accuracy improvement over the state of the art method demonstrating the benefits in practical applications We formulate the statistical path selection problem for at speed test as a gambling problem and present an elegant solution based on the Kelly criterion To circumvent the coverage loss issue in statistical path selection we propose a testability driven approach making it a practical solution for coping with parametric defects *Electrical & Electronics Abstracts* ,1997 **Constraining Designs for Synthesis and Timing Analysis** Sridhar Gangadharan,Sanjay Churiwala,2015-06-23 This book serves as a hands on guide to timing constraints in integrated circuit design Readers will learn to maximize performance of their IC designs by

specifying timing requirements correctly Coverage includes key aspects of the design flow impacted by timing constraints including synthesis static timing analysis and placement and routing Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow all within the context of Synopsys Design Constraints SDC the industry leading format for specifying constraints

A Linear-time Approach for Static Timing Analysis

Covering All Process Corners Sari Onaissi,2007 Manufacturing process variations lead to circuit timing variability and a corresponding timing yield loss Traditional corner analysis consists of checking all process corners combinations of process parameter extremes to make sure that circuit timing constraints are met at all corners typically by running static timing analysis STA at every corner This approach is becoming too expensive due to the increase in the number of corners with modern processes As an alternative we propose a linear time approach for STA which covers all process corners in a single pass Our technique assumes a linear dependence of delays and slews on process parameters and provides tight bounds on the worst case circuit delay and slew It exhibits high accuracy up to 2% in practice and if the circuit has m gates and n relevant process parameters the complexity of the algorithm is $O(mn)$

Timing Analysis of Real-time Software L. Motus,M. G. Rodd,1994 a practical approach to the specification and design of real time embedded software with an emphasis on timing correctness The method uses the Q model a technique which adds explicit timing parameters to data flow or object modeling diagrams supported by a flexible time selective process interaction mechanism

Static timing analysis A Complete Guide Gerardus Blokdyk,2018 Static timing analysis A Complete Guide

Timing Sachin Sapatnekar,2007-05-08 Statistical timing analysis is an area of growing importance in nanometer technologies as the uncertainties associated with process and environmental variations increase and this chapter has captured some of the major efforts in this area This remains a very active field of research and there is likely to be a great deal of new research to be found in conferences and journals after this book is published In addition to the statistical analysis of combinational circuits a good deal of work has been carried out in analyzing the effect of variations on clock skew Although we will not treat this subject in this book the reader is referred to LNPS00 HN01 JH01 ABZ03a for details

7 TIMING ANALYSIS FOR SEQUENTIAL CIRCUITS

7.1 INTRODUCTION A general sequential circuit is a network of computational nodes gates and memory elements registers The computational nodes may be conceptualized as being clustered together in an acyclic network of gates that forms a combinational logic circuit A cyclic path in the direction of signal propagation is permitted in the sequential circuit only if it contains at least one register In general it is possible to represent any sequential circuit in terms of the schematic shown in Figure 7.1 which has I inputs O outputs and M registers The registers outputs feed into the combinational logic which in turn feeds the register inputs Thus the combinational logic has I M inputs and O M outputs

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