Chapter 3 Solutions

1 a) $I_D = \dfrac{V_{in} - 2V_{Don}}{R_1 + R_2}$

$= \dfrac{2.5 - 1.4}{4k\Omega} = \dfrac{1.1V}{4k\Omega}$

$$\boxed{I_D = 275\mu A}$$

b) $I_S = 10^{14}A$, $T = 300K$, $V_{Don} = 0.7V$

$I_D = I_S(e^{V_D/\phi_T} - 1)$

where $\phi_T = \dfrac{kT}{q} = 26mV$ @ 300 K

(A) $I_o = \dfrac{V_{in} - 2V_D}{R_1 + R_2} = I_S(e^{V_D/\phi_T} - 1)$

$\dfrac{2.5 - 2V_D}{4k\Omega} = 10^{14}(e^{V_D/.026} - 1)$

iterating on this expression
we can obtain

$$\boxed{V_D = 0.628V}$$
$$\boxed{I_o = 311\mu A}$$

c) SPICE

exercise 3.1
vin in 0 dc 2.5
r1 in 2 2k
d1 2 3 D
r2 3 out 2k
d2 out 0 D

.options post=2
.op

.model D D level=1 is=1e-14 n=0.5
.end
****
NODE   VOLTAGE
2   1.8750E+00
3   1.2500E+00
OUT   6.2501E-01

CURRENT   3.1269E-04

d) $I_S = 10^{-16}A$, $T = 300K$;
again use (A) from b and iterate
to find

$$\boxed{\begin{array}{l} V_D = 0.743V \\ I_D = 253\mu A \end{array}}$$

$I_S = 10^{14}A$, $T = 350K$;

$$\boxed{\begin{array}{l} V_D = 0.728V \\ I_D = 261\mu A \end{array}}$$

exercise 3.1d
vin in 0 dc 2.5
r1 in 2 2k
d1 2 3 D
r2 3 out 2k
d2 out 0 D

.options post=2
.op

*.temp27
.temp 77
*.model D D level=1 is=1e-16 n=0.5
.model D D level=1 is=1e-14 n=0.5
.end
****
t=27C
NODE   VOLTAGE
2   1.9889E+00
3   1.2500E+00
IN   2.5000E+00
OUT   7.2892E-01

ID   2.5554E-04
****
t=77C
NODE   VOLTAGE
2   1.7844E+00
3   1.2500E+00
IN   2.5000E+00
OUT   5.3436E-01

ID   3.5782E-04

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Jan Rabaey Staff

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Low-Power Electronics Design Christian Piguet,2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today s methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now   Low-Power Processors and Systems on Chips Christian Piguet,2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet s recently published Low Power Electronics Design this volume addresses the design of low power microprocessors in deep submicron technologies It provides a focused reference for specialists involved in systems on chips from low power microprocessors to DSP cores reconfigurable processors memories ad hoc networks and embedded software Low Power Processors and Systems on Chips is organized into three broad sections for convenient access The first section examines the design of digital signal processors for embedded applications and techniques for reducing dynamic and static power at the electrical and system levels The second part describes several aspects of low power systems on chips including hardware and embedded software aspects efficient data storage networks on chips and applications such as routing strategies in wireless RF sensing and actuating devices The final section discusses embedded software issues including details on compilers retargetable compilers and coverification tools Providing detailed examinations contributed by leading experts Low Power Processors and Systems on Chips supplies authoritative information on how to maintain high performance while lowering power consumption in modern processors and SoCs It is a must read for anyone designing modern computers or embedded systems

Transforming Tomorrow: Innovative Solutions and Global Trends in Electrical and Electronics Engineering Namit Gupta,Anjali Gupta,Naresh Purohit,Shiraz Husain,2025-06-03 The International Conference on Transforming Tomorrow Innovative Solutions and Global Trends in Electrical and Electronics Engineering Pragyata 2025 is scheduled to be held on May 5 6 2025 at Shri Vaishnav Vidyapeeth Vishwavidyalaya Indore Madhya Pradesh India This prestigious event aims to provide a dynamic platform for researchers academicians industry professionals and students to exchange knowledge

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Chu,2012-05-14 Explores the unique hardware programmability of FPGA based embedded systems using a learn by doing approach to introduce the concepts and techniques for embedded SoPC design with Verilog An SoPC system on a programmable chip integrates a processor memory modules I O peripherals and custom hardware accelerators into a single FPGA field programmable gate array device In addition to the customized software customized hardware can be developed and incorporated into the embedded system as well allowing us to configure the soft core processor create tailored I O interfaces and develop specialized hardware accelerators for computation intensive tasks Utilizing an Altera FPGA prototyping board and its Nios II soft core processor Embedded SoPC Design with Nios II Processor and Verilog Examples takes a learn by doing approach to illustrate the hardware and software design and development process by including realistic projects that can be implemented and tested on the board Emphasizing hardware design and integration throughout the book is divided into four major parts Part I covers HDL and synthesis of custom hardware Part II introduces the Nios II processor and provides an overview of embedded software development Part III demonstrates the design and development of hardware and software of several complex I O peripherals including a PS2 keyboard and mouse a graphic video controller an audio codec and an SD secure digital card Part IV provides several case studies of the integration of hardware accelerators including a custom GCD greatest common divisor circuit a Mandelbrot set fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology While designing and developing an embedded SoPC can be rewarding the learning can be a long and winding journey This book shows the trail ahead and guides readers through the initial steps to exploit the full potential of this emerging methodology   FPGA Prototyping by VHDL Examples Pong P. Chu,2011-09-20 This book uses a learn by doing approach to introduce the concepts and techniques of VHDL and FPGA to designers through a series of hands on experiments FPGA Prototyping by VHDL Examples provides a collection of clear easy to follow templates for quick code development a large number of practical examples to illustrate and reinforce the concepts and design techniques realistic projects that can be implemented and tested on a Xilinx prototyping board and a thorough exploration of the Xilinx PicoBlaze soft core microcontroller   **Solutions Manual** Jan Rabaey Staff,   VLSI Signal Processing, VII Jan Rabaey,Paul M. Chau,John Eldon,1994   Mergent International Manual ,2003   *14th Symposium on Integrated Circuits and Systems Design* Sociedade Brasileira de Computação,2001 Annotation Papers from a September 2001 symposium report on recent advances in areas of integrated circuits and systems design including embedded systems rapid prototyping formal methods codesign CAD and test analog digital and physical design and low power and low voltage Specific topics include communication architectures for system on chip using the CAN protocol and reconfigurable computing technology for Web based smart house automation and optimizing BBD based verification analyzing variable dependencies Other subjects include interconnection length estimation at logic level an environment to aid the synthesis of threephase analogue waveform using AHDL and extending sequencing graphs for reconfigurable applications modeling This work lacks a subject index c Book

News Inc   The Proceedings of the European Design Automation Conference ,1990   **Digest of Technical Papers** ,2001
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