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Substrate Noise Coupling in RFICs

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Substrate Noise Coupling In Rfics Analog Circuits And Signal Processing:

Substrate Noise Coupling in RFICs Ahmed Helmy,Mohammed Ismail,2008-03-23 The book reports modeling and simulation techniques for substrate noise coupling effects in RFICs and introduces isolation structures and design guides to mitigate such effects with the ultimate goal of enhancing the yield of RF and mixed signal SoCs The book further reports silicon measurements and new test and noise isolation structures To the authors knowledge this is the first title devoted to the topic of substrate noise coupling in RFICs as part of a large SoC *Substrate Noise Coupling in Mixed-Signal ASICs* Stéphane Donnay,Georges Gielen,2003-02-28 Driven by applications such as telecommunications computing and consumer multimedia and facilitated by the progress in CMOS ULSI technology the microelectronics IC market is characterized by an ever increasing level of integration complexity Today complete systems that previously occupied one or more boards are integrated on a few chips or even on one single multi million transistor chip a so called System on Chip SoC Although most functions in such integrated systems are implemented with digital or digital signal processing circuitry the analog circuits needed at the interface between the electronic system and the continuous valued outside world are also being integrated on the same die for reasons of cost and performance Unfortunately the integration of both analog RF circuits and digital circuits on the same die not only offers many benefits but also creates some technical difficulties Since the analog circuits exploit the low level physics of the fabrication process they remain difficult and costly to design but they are also vulnerable to any kind of noise or crosstalk signals The higher levels of integration moving towards 100 million transistors per chip clocked at ever higher frequencies make the mixed signal signal integrity problem increasingly challenging One of the most important problems is the parasitic supply and substrate noise coupling caused by the fast switching of the digital circuitry that then propagates to the sensitive analog circuitry via the common substrate It is therefore important to be able to predict the impact of digital switching noise on the analog circuit performance at the design stage of the integrated system before the chip is taped out for fabrication and to understand how this problem can be reduced The purpose of Substrate Noise Coupling in Mixed Signal ASICs is to provide an overview of very recent research results in the field of substrate noise analysis and reduction techniques Much of the reported work has been established as part of the Mixed Signal Initiative of the European Union It is a representative sampling of the current state of the art in this area All the different aspects of the substrate noise coupling problem are covered Some chapters describe techniques to model and reduce the digital switching noise injected in the substrate Other chapters describe methods to analyse the propagation of the noise from the source the digital circuitry to the reception point the embedded analog circuitry through the substrate considered as a resistive capacitive mesh Finally the remaining chapters describe techniques to model and especially to reduce the impact of substrate noise on the analog side This is illustrated with several practical design examples and measurement results

Noise Coupling in System-on-Chip Thomas Noulis,2018-01-09 Noise Coupling is the root cause of the majority of

Systems on Chip SoC product fails The book discusses a breakthrough substrate coupling analysis flow and modelling toolset addressing the needs of the design community The flow provides capability to analyze noise components propagating through the substrate the parasitic interconnects and the package Using this book the reader can analyze and avoid complex noise coupling that degrades RF and mixed signal design performance while reducing the need for conservative design practices With chapters written by leading international experts in the field novel methodologies are provided to identify noise coupling in silicon It additionally features case studies that can be found in any modern CMOS SoC product for mobile communications automotive applications and readout front ends Characterization of Substrate Noise Coupling, Its Impacts and Remedies in RF and Mixed-signal ICs Ahmed Helmy,2006 Abstract Substrate noise coupling in integrated circuits is the process by which interference signals generated by high speed digital blocks cause parasitic currents to flow in the silicon substrate and couple devices in various parts of the circuits on this common substrate In RFIC the switching noise couples to the sensitive analog circuits through the substrate causing degradation in performance and yield hit Overcoming substrate coupling is a key issue in successful system on chip integration In this thesis a substrate aware design flow is built calibrated to silicon and used as part of the design flow to uncover substrate coupling problems in RFICs in the design phase The flow is used to develop the first comprehensive RF substrate noise isolation design guide to be used by RF designers during the design phase This will allow designers to optimize the design to maximize noise isolation and protect sensitive blocks from being degraded by substrate noise coupling Several effects of substrate coupling on circuit performance will be identified and remedies will be given based on the design guide Three case studies are designed to analyze the substrate coupling problem in RFICs The case studies are designed to attack the problem from the device circuit and system levels On the device level a special emphasis is given to designing on chip inductors as an important device in RFIC An accurate model is developed for a broadband fit of the inductor scattering parameters This model is shown to be scalable and is proven to be accurate across various frequency bands and geometries A special emphasis is put on the design for manufacturing effects that affect the design robustness A circuit level case study is developed and results are compared to simulations and measurements to highlight the need for such a flow before tapping out to ensure a yielding part The system level problem studied is a GSM receiver where the research results are directly applied to it as a demonstration vehicle to debug and resolve a system level substrate noise coupling problem that otherwise caused a product to be on the edge of malfunction

Omnidirectional Inductive Powering for Biomedical Implants Bert Lenaerts,Robert Puers,2008-10-14 Omnidirectional Inductive Powering for Biomedical Implants investigates the feasibility of inductive powering for capsule endoscopy and freely moving systems in general The main challenge is the random position and orientation of the power receiving system with respect to the emitting magnetic field Where classic inductive powering assumes a predictable or fixed alignment of the respective coils the remote system is now free to adopt just any orientation while still maintaining full power

capabilities Before elaborating on different approaches towards omnidirectional powering the design and optimisation of a general inductive power link is discussed in all its aspects Special attention is paid to the interaction of the inductive power link with the patient s body Putting theory into practice the implementation of an inductive power link for a capsule endoscope is included in a separate chapter **EDA for IC Implementation, Circuit Design, and Process Technology** Luciano Lavagno,Louis Scheffer,Grant Martin,2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The second volume EDA for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic to GDSII a file format used to transfer data of semiconductor physical layout analog mixed signal design physical verification and technology CAD TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale power supply network design and analysis design modeling and much more Save on the complete set Low Power UWB CMOS Radar Sensors Hervé Paulino,Joao Goes,Adolfo Steiger Garção,2008-04-30 Low Power UWB CMOS Radar Sensors deals with the problem of designing low cost CMOS radar sensors The radar sensor uses UWB signals in order to obtain a reasonable target separation capability while maintaining a maximum signal frequency below 2 GHz This maximum frequency value is well within the reach of current CMOS technologies The use of UWB signals means that most of the methodologies used in the design of circuits and systems that process narrow band signals can no longer be applied Low Power UWB CMOS Radar Sensors provides an analysis between the interaction of UWB signals the antennas and the processing circuits This analysis leads to some interesting conclusions on the types of antennas and types of circuits that should be used A methodology to compare the noise performance of UWB processing circuits is also derived This methodology is used to analyze and design the constituting circuits of the radar transceiver In order to validate the design methodology a CMOS prototype is designed and experimentally evaluated *Low-Power High-Speed ADCs for Nanometer CMOS Integration* Zhiheng Cao,Shouli Yan,2008-07-15 Low Power High Speed ADCs for Nanometer CMOS Integration is about the design and implementation of ADC in nanometer CMOS processes that achieve lower power consumption for a given speed and resolution than previous designs through architectural and circuit innovations that take advantage of unique features of nanometer CMOS processes A phase lock loop PLL clock multiplier has also been designed using new circuit techniques and successfully tested 1 A 1 2V 52mW 210MS s 10 bit two step ADC in 130nm CMOS occupying 0 38mm2 Using offset canceling comparators and capacitor networks implemented with small value interconnect capacitors to replace resistor ladder multiplexer in conventional sub ranging ADCs it achieves 74dB SFDR for 10MHz and 71dB SFDR for 100MHz input 2 A 32mW 1 25GS s 6 bit ADC with 2 5GHz internal clock in 130nm CMOS A new type of architecture that combines flash and SAR enables the lowest power consumption 6 bit 1GS s ADC reported to date This design can be a drop in replacement for existing flash ADCs since it does

require any post processing or calibration step and has the same latency as flash 3 A 0 4ps rms jitter integrated from 3kHz to 300MHz offset for 2 5GHz 1 3GHz tunable phase noise programmable clock multiplier PLL for generating sampling clock to the SAR ADC A new loop filter structure enables phase error preamplification to lower PLL in band noise without increasing loop filter capacitor size **Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology** Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

Substrate Noise Coupling in Analog/RF Circuits Stephane Bronckers,Geert Van der Plas,Gerd Vandersteen,Yves Rolain,2010 This book presents case studies to illustrate that careful modeling of the assembly characteristics and layout details is required to bring simulations and measurements into agreement Engineers learn how to use a proper combination of isolation structures and circuit techniques to make analog RF circuits more immune to substrate noise Topics include substrate noise propagation passive isolation structures noise couple in active devices measuring the coupling mechanisms in analog RF circuits prediction of the impact of substrate noise on analog RF circuits and noise coupling in analog RF systems

Dissertation Abstracts International ,2007 **Technologies Enabling Future Mobile Connectivity & Sensing** Björn Debaillie,François Brunier,Dominique Morche,Erkan Nevzat Isa,Jan Craninckx,2024-01-09 In today s connected world the demand for mobile communications and instant access to information anytime and anywhere has drastically changed the electronics landscape both consumer and industrial Novel 5G and 6G systems will enable connectivity in all forms between humans devices machines and any objects They will provide virtually ubiquitous ultra high bandwidth and low latency network access to individual users as well as to all objects benefiting from being connected They will be the eyes and ears of Artificial Intelligence systems as it will provide real time data collection and analysis Such diversity calls for a new paradigm

in terms of flexibility not only related to performance but also in terms of scalability and cost 5G and 6G communication systems imply a major stake of sovereignty and autonomy for the communication sector and digital infrastructures of the future All products related to IoT traffic and health care supported by connectivity will benefit the citizens in their daily lives to improve everything from business to private affairs Together this will influence society as much as smart phones did in the recent past It is all about communication and connectivity This book provides an overview of the latest research results in this field It is based on the close collaboration in the BEYOND5 project extended with vision and roadmap insights by European experts leading the 6G development The BEYOND5 project has built a completely European supply chain for Radio Frequency Electronics enabling new RF domains for sensing communication 5G radio infrastructure and beyond Moving forward into higher frequency bands above 100 GHz for 6G also more disruptive technologies using heterogeneous integration of CMOS SOI and III V components such as GaN or InP and advanced packaging techniques will be necessary to realize the objectives of ubiquitous ultra high bandwidth and low latency networks The book bundles the scientific content of the International Workshop on Technologies enabling future mobile connectivity sensing in Lisbon Portugal 10 September 2023 as part of the ESSCIRC ESSDERC 2023 European Solid state Circuits and Devices Conference Through articles and abstracts a combined view of experts and practitioners representing academia research and industry in the field of wireless communication systems is given They cover the topics of RF and digital SOI technology development for 5 and 6G device and substrate characterization packaging technology and the realization of full systems including power amplifiers linearization techniques beamforming transceivers access points and radar detection *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs* X. Aragones,J.L. Gonzalez,Antonio Rubio,2013-03-09 Modern microelectronic design is characterized by the integration of full systems on a single die These systems often include large high performance digital circuitry high resolution analog parts high driving I O and maybe RF sections Designers of such systems are constantly faced with the challenge to achieve compatibility in electrical characteristics of every section some circuitry presents fast transients and large consumption spikes whereas others require quiet environments to achieve resolutions well beyond millivolts Coupling between those sections is usually unavoidable since the entire system shares the same silicon substrate bulk and the same package Understanding the way coupling is produced and knowing methods to isolate coupled circuitry and how to apply every method is then mandatory knowledge for every IC designer Analysis and Solutions for Switching Noise Coupling in Mixed Signal ICs is an in depth look at coupling through the common silicon substrate and noise at the power supply lines It explains the elementary knowledge needed to understand these phenomena and presents a review of previous works and new research results The aim is to provide an understanding of the reasons for these particular ways of coupling review and suggest solutions to noise coupling and provide criteria to apply noise reduction Analysis and Solutions for Switching Noise Coupling in Mixed Signal ICs is an ideal book both as introductory material to noise coupling problems in

mixed signal ICs and for more advanced designers facing this problem **Analysis of Substrate Noise Coupling in Mixed Signal Integrated Circuits** Cole Erwin Zemke,2003 **Deutsche Nationalbibliographie und Bibliographie der im Ausland erschienenen deutschsprachigen Veröffentlichungen** ,2009 **Modeling of Substrate Noise Coupling in Mixed-signal Integrated Circuits** Nawej Mwez,2002 Microwave Journal ,2006 **Substrate Noise Analysis in RF Integrated Circuits** ,2004 Substrate coupling in integrated circuits is the process whereby parasitic current flow in the substrate electrically couples devices in different parts of the circuit Higher levels of integration and higher frequencies of operation makes the coupling more pronounced in modern circuit realizations Electrical coupling in the substrate leads to undesirable interaction between devices which can degrade circuit performance The degradation can manifest itself in different ways In mixed analog digital circuits for example the switching noise generated by digital circuits can be coupled to sensitive analog circuits through the substrate Performance degradation due to substrate coupling can be addressed at the circuit design stage by including substrate models in circuit analysis Analytical models based on simple substrate resistance plots are developed Trends in substrate resistance variation for different substrates are studied to understand its effect at the circuit level Analytical model for measurement of substrate coupling at the circuit level based on substrate resistance information and other circuit parameters is developed Efficient techniques to improve isolation based on simulation and analysis of the substrate model are discussed **Resistive Model of Substrate Noise Coupling in Mixed Signal Circuits** Hongmei Li,2002 *Substrate Coupling in Mixed Signal IC's* Elie M. Issa,Prairie View A & M University. Graduate School,2007 Integrating digital with sensitive analog circuitry has created concerns for signal integrity The fast switching digital signal creates noise that injects through the doped silicon substrate abd travels through it due to its low resistivity to the analog circuits causing damages and operational bandwidth reduction How much is the coupling and how to control it These are the questions that will be answered in this thesis using 3D filed solver COMSOL to extract the substrate coupling parameters v

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