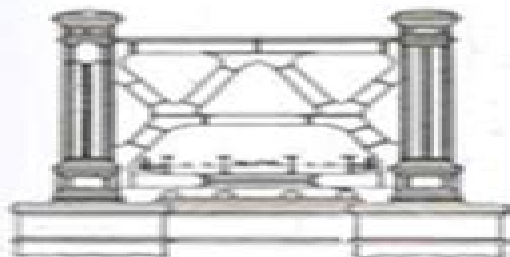
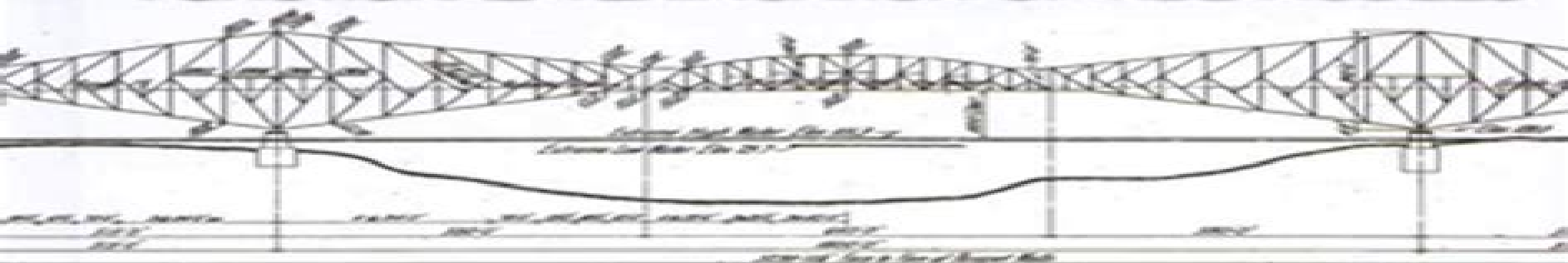


Writing Testbenches

FUNCTIONAL VERIFICATION OF HDL MODELS



by Janick Bergeron



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Writing Testbenches Functional Verification Of Hdl Models

Janick Bergeron



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mental improvements during the same period What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough In the second edition of Writing Testbenches Bergeron raises the verification level of abstraction by introducing coverage driven constrained random transaction level self checking testbenches all made possible through the introduction of hardware verification languages HVLs such as e from Verisity and OpenVera from Synopsys The state of art methodologies described in Writing Test benches will contribute greatly to the much needed equivalent of a synthesis breakthrough in verification productivity I not only highly recommend this book but also I think it should be required reading by anyone involved in design and verification of today s ASIC SoCs and systems Harry Foster Chief Architect Verplex Systems Inc xviii Writing Testbenches Functional Verification of HDL Models PREFACE If you survey hardware design groups you will learn that between 60% and 80% of their effort is now dedicated to verification

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Verification Methodology Manual for SystemVerilog Janick Bergeron,Eduard Cerny,Alan Hunter,Andy Nightingale,2005-09-28 Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly Unique in its broad coverage of SystemVerilog advanced functional verification and the combination of the two

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 available tools and provide hands on experience with the design tools Review questions and problems are given at the end of
 each chapter to revise the concepts Recent trends and references are listed at the end of each chapter for further reading

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Engineering Materials, Energy, Management and Control Zhihua Xu,Gang Shen,Sally Lin,2010-12-06 Selected peer reviewed papers of the 2011 International Conference on Engineering Materials Energy Management and Control MEMC 2011 January 22 23 2011 Beijing P R China

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Functional Design Error Diagnosis, Correction and Layout Repair of Digital Circuits Kai-Hui Chang,2007 *18th International Conference on VLSI Design* International Conference on VLSI Design,2005

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