Synopsys Design Compiler Documents

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Synopsys Design Compiler User Guide

AW Rasmussen

Synopsys Design Compiler User Guide:

   Design of Energy-Efficient Application-Specific Instruction Set Processors Tilman Glökler,Heinrich Meyr,2007-05-08 After a brief introduction to low power VLSI design the design space of ASIP instruction set architectures ISAs is introduced with a special focus on important features for digital signal processing Based on the degrees of freedom offered by this design space a consistent ASIP design flow is proposed this design flow starts with a given application and uses incremental optimization of the ASIP hardware of ASIP coprocessors and of the ASIP software by using a top down approach and by applying application specific modifications on all levels of design hierarchy A broad range of real world signal processing applications serves as vehicle to illustrate each design decision and provides a hands on approach to ASIP design Finally two complete case studies demonstrate the feasibility and the efficiency of the proposed methodology and quantitatively evaluate the benefits of ASIPs in an industrial context   *Transaction-Level Power Modeling* Amr Baher Darwish,Magdy Ali El-Moursy,Mohamed Amin Dessouky,2019-08-01 This book describes for readers a methodology for dynamic power estimation using Transaction Level Modeling TLM The methodology exploits the existing tools for RTL simulation design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling TLPM Readers will benefit from this innovative way of evaluating power on a high level of abstraction at an early stage of the product life cycle decreasing the number of the expensive design iterations   Digital Logic Design Using Verilog Vaibbhav Taraate,2021-10-31 This second edition focuses on the thought process of digital design and implementation in the context of VLSI and system design It covers the Verilog 2001 and Verilog 2005 RTL design styles constructs and the optimization at the RTL and synthesis level The book also covers the logic synthesis low power multiple clock domain design concepts and design performance improvement techniques The book includes 250 design examples illustrations and 100 exercise questions This volume can be used as a core or supplementary text in undergraduate courses on logic design and as a text for professional and vocational coursework In addition it will be a hands on professional reference and a self study aid for hobbyists   **Closing the Power Gap between ASIC & Custom** David Chinnery,Kurt Keutzer,2008-01-23 Explains how to use low power design in an automated design flow and examine the design time and performance trade offs Includes the latest tools and techniques for low power design applied in an ASIC design flow Focuses on low power in an automated design methodology a much neglected area   **Emerging Memory and Computing Devices in the Era of Intelligent Machines** Pedram Khalili Amiri,2020-04-16 Computing systems are undergoing a transformation from logic centric towards memory centric architectures where overall performance and energy efficiency at the system level are determined by the density performance functionality and efficiency of the memory rather than the logic sub system This is driven by the requirements of data intensive applications in artificial intelligence autonomous systems and edge computing We are at an exciting time in the semiconductor industry where several innovative device and technology

concepts are being developed to respond to these demands and capture shares of the fast growing market for AI related hardware This special issue is devoted to highlighting discussing and presenting the latest advancements in this area drawing on the best work on emerging memory devices including magnetic resistive phase change and other types of memory The special issue is interested in work that presents concepts ideas and recent progress ranging from materials to memory devices physics of switching mechanisms circuits and system applications as well as progress in modeling and design tools Contributions that bridge across several of these layers are especially encouraged   <u>Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation</u> Vassilis Paliouras,Johan Vounckx,Diederik Verkest,2005-08-25 Welcome to the proceedings of PATMOS 2005 the 15th in a series of international workshops PATMOS2005wasorganizedbyIMECwithtechnicalco sponsorshipfrom the IEEE Circuits and Systems Society Over the years PATMOS has evolved into an important European event where searchers from both industry and academia discuss and investigate the emerging ch lenges in future and contemporary applications design methodologies and tools quired for the developmentof upcominggenerationsof integrated circuits and systems The technical program of PATMOS 2005 contained state of the art technical contri tions three invited talks a special session on hearing aid design and an embedded torial The technical program focused on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design char terization analysis and optimization in the nanometer era The Technical Program Committee with the assistance of additional expert revi ers selected the 74 papers to be presented at PATMOS The papers were divided into 11 technical sessions and 3 poster sessions As is always the case with the PATMOS workshops the review process was anonymous full papers were required and several reviews were carried out per paper Beyond the presentations of the papers the PATMOS technical program was riched by a series of speeches offered by world class experts on important emerging research issues of industrial relevance Prof Jan Rabaey Berkeley USA gave a talk on Traveling the Wild Frontier of Ulta Low Power Design Dr Sung Bae Park S sung gave a presentation on DVL Deep Low Voltage Circuits and Devices Prof

Field-programmable Logic and Applications ,2002   **Hardware/Software Co-Design** Giovanni DeMicheli,M.G. Sami,2013-11-11 Concurrent design or co design of hardware and software is extremely important for meeting design goals such as high performance that are the key to commercial competitiveness Hardware Software Co Design covers many aspects of the subject including methods and examples for designing 1 general purpose and embedded computing systems based on instruction set processors 2 telecommunication systems using general purpose digital signal processors as well as application specific instruction set processors 3 embedded control systems and applications to automotive electronics The book also surveys the areas of emulation and prototyping systems with field programmable gate array technologies hardware software synthesis and verification and industrial design trends Most contributions emphasize the design methodology the requirements and state of the art of computer aided co design tools together with current design examples   *FPGA ...* ,2006

Low Power Design Automation David Graeme Chinnery,2006 **Proceedings** ,2004 *Integration of Dual-edge Triggered Clocked Storage Elements Into a Synthesizable Microprocessor Core* Gabriel Rui René Johnson Ricardo,2004 Energy Scalable Distributed Arithmetic on a Field Programmable Gate Array and a Standard-cell Core Zulfiqar Ali Ansari,2005 **Integrated Circuit and System Design** ,2005 **Method Integration** Klaus Kronlöf,1993 Using a systematic approach it describes the concept of method integration Presents a detailed investigation of several major techniques including Information Modeling Structured Analysis and VHDL stressing their integration Also describes company specific or research methods that provide distinctive and theoretically advanced features such as HIT and COLD Contains case studies on Siemens Daimler Benz and Philips which illustrate the ideas introduced *IEEE Symposium on FPGAs for Custom Computing Machines* Kenneth L. Pocek,Jeffrey M. Arnold,1996 Contains papers from the April 1996 symposium reporting on research in device architectures applications compilers and related software support Topics include using MORRPH in an industrial machine vision system a software development system for FPGA based data acquisition systems a reconfigura Digital Architecture for High Resolution Micro-simulator for Retinal Prosthesis Linh Hoàng,2007 **High Throughput VLSI Architectures for Iterative Decoders** Engling Yeo,2003 18th International Conference on VLSI Design International Conference on VLSI Design,2005 **Annual Meeting of the North American Fuzzy Information Processing Society--NAFIPS.** North American Fuzzy Information Processing Society. Annual Meeting,1997

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