

Kazuo Kondo · Masahiro Kado
Kenji Takahashi Editors

Three- Dimensional Integration of Semiconductors

Processing, Materials, and Applications



Springer

Three Dimensional Integration Semiconductors Processing Applications

Katsuyuki Sakuma



Three Dimensional Integration Semiconductors Processing Applications:

Three-Dimensional Integration of Semiconductors Kazuo Kondo, Morihiro Kada, Kenji Takahashi, 2015-12-09 This book starts with background concerning three dimensional integration including their low energy consumption and high speed image processing and then proceeds to how to construct them and which materials to use in particular situations The book covers numerous applications including next generation smart phones driving assistance systems capsule endoscopes homing missiles and many others The book concludes with recent progress and developments in three dimensional packaging as well as future prospects

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Handbook of 3D Integration, Volume 1 Philip Garrou, Christopher Bower, Peter Ramm, 2011-09-22 The first encompassing treatise of this new but very important field puts the known physical limitations for classic 2D electronics into perspective with the requirements for further electronics developments and market necessities This two volume handbook presents 3D solutions to the feature density problem addressing all important issues such as wafer processing die bonding packaging technology and thermal aspects It begins with an introductory part which defines necessary goals existing issues and relates 3D integration to the semiconductor roadmap of the industry Before going on to cover processing technology and 3D structure fabrication strategies in detail This is followed by fields of application and a look at the future of 3D integration The contributions come from key players in the field from both academia and industry including such companies as Lincoln Labs Fraunhofer RPI ASET IMEC CEA LETI IBM and Renesas

Semiconductor Wafer Bonding VII : Science, Technology, and Applications ,2003 *Simulation of Semiconductor Processes and Devices 1998* Kristin De Meyer, Serge Biesemans, 1998-08-17 This volume contains the proceedings of the 1998 International Conference on Simulation of Semiconductor Processes and Devices and provides an open forum for the presentation of the latest results and trends in modeling and simulation of semiconductor equipment processes and devices Topics include semiconductor equipment simulation process modeling and simulation device modeling and simulation of complex structures interconnect modeling integrated systems for process device circuit simulation and optimisation numerical methods and algorithms compact modeling and parameter extraction modeling for RF applications simulation and modeling of new devices heterojunction based SET s quantum effect devices laser based

Scientific and Technical Aerospace Reports ,1993 Three Dimensional System Integration Antonis Papanikolaou, Dimitrios Soudris, Riko Radojcic, 2010-12-07 Three dimensional 3D integrated circuit IC stacking is the next big step in electronic system integration

It enables packing more functionality as well as integration of heterogeneous materials devices and signals in the same space volume This results in consumer electronics e g mobile handheld devices which can run more powerful applications such as full length movies and 3D games with longer battery life This technology is so promising that it is expected to be a mainstream technology a few years from now less than 10 15 years from its original conception To achieve this type of end product changes in the entire manufacturing and design process of electronic systems are taking place This book provides readers with an accessible tutorial on a broad range of topics essential to the non expert in 3D System Integration It is an invaluable resource for anybody in need of an overview of the 3D manufacturing and design chain

Wafer Level 3-D ICs Process Technology Chuan Seng Tan, Ronald J. Gutmann, L. Rafael Reif, 2009-06-29 Three dimensional 3D integration is clearly the simplest answer to most of the semiconductor industry s vexing problems heterogeneous integration and reductions of power form factor delay and even cost Conceptually the power latency and form factor of a system with a fixed number of transistors all scale roughly linearly with the diameter of the smallest sphere enclosing frequently interacting devices This clearly provides the fundamental motivation behind 3D technologies which vertically stack several strata of device and interconnect layers with high vertical interconnectivity In addition the ability to vertically stack strata with divergent and even incompatible process flows provides for low cost and low parasitic integration of diverse technologies such as sensors energy scavengers nonvolatile memory dense memory fast memory processors and RF layers These capabilities coupled with today s trends of increasing levels of integrated functionality lower power smaller form factor increasingly divergent process flows and functional diversification would seem to make 3D technologies a natural choice for most of the semiconductor industry Since the concept of vertical integration of different strata has been around for over 20 years why aren t vertically stacked strata endemic to the semiconductor industry The simple answer to this question is that in the past the 3D advantages while interesting were not necessary due to the tremendous opportunities offered by geometric scaling In addition even when the global interconnect problem of high performance single core processors seemed insurmountable without innovations such as 3D alternative architectural solutions such as multicores could effectively delay but not eliminate the need for 3D

IBM Journal of Research and Development ,2006

3D Integration in VLSI Circuits Katsuyuki Sakuma, 2018-04-17 Currently the term 3D integration includes a wide variety of different integration methods such as 2.5 dimensional 2.5D interposer based integration 3D integrated circuits 3D ICs 3D systems in package SiP 3D heterogeneous integration and monolithic 3D ICs The goal of this book is to provide readers with an understanding of the latest challenges and issues in 3D integration TSVs are not the only technology element needed for 3D integration There are numerous other key enabling technologies required for 3D integration and the speed of the development in this emerging field is very rapid To provide readers with state of the art information on 3D integration research and technology developments each chapter has been contributed by some of the world s leading scientists and experts from academia research institutes and industry from around the globe Covers chip

wafer level 3D integration technology memory stacking reconfigurable 3D and monolithic 3D IC Discusses the use of silicon interposer and organic interposer Presents architecture design and technology implementations for 3D FPGA integration Describes oxide bonding Cu SiO₂ hybrid bonding adhesive bonding and solder bonding Addresses the issue of thermal dissipation in 3D integration **Handbook of 3D Integration, Volume 3** Philip Garrou, Mitsumasa Koyanagi, Peter Ramm, 2014-07-21 Edited by key figures in 3D integration and written by top authors from high tech companies and renowned research institutions this book covers the intricate details of 3D process technology As such the main focus is on silicon via formation bonding and debonding thinning via reveal and backside processing both from a technological and a materials science perspective The last part of the book is concerned with assessing and enhancing the reliability of the 3D integrated devices which is a prerequisite for the large scale implementation of this emerging technology Invaluable reading for materials scientists semiconductor physicists and those working in the semiconductor industry as well as IT and electrical engineers 3D IC Stacking Technology Banqiu Wu, Ajay Kumar, Sesh Ramaswami, 2011-10-14 The latest advances in three dimensional integrated circuit stacking technology With a focus on industrial applications 3D IC Stacking Technology offers comprehensive coverage of design test and fabrication processing methods for three dimensional device integration Each chapter in this authoritative guide is written by industry experts and details a separate fabrication step Future industry applications and cutting edge design potential are also discussed This is an essential resource for semiconductor engineers and portable device designers 3D IC Stacking Technology covers High density through silicon stacking TSS technology Practical design ecosystem for heterogeneous 3D IC products Design automation and TCAD tool solutions for through silicon via TSV based 3D IC stack Process integration for TSV manufacturing High aspect ratio silicon etch for TSV Dielectric deposition for TSV Barrier and seed deposition Copper electrodeposition for TSV Chemical mechanical polishing for TSV applications Temporary and permanent bonding Assembly and test aspects of TSV technology **Conference Proceedings**, 1993 **Fiftieth Anniversary, 1912-1962** Institute of Radio Engineers, 1962 **1975 IEEE International Solid-State Circuits Conference**, 1975 Annual IEEE Semiconductor Thermal Measurement and Management Symposium, 1998 **An Introductory Guide to EC Competition Law and Practice** Valentine Korah, 1994 *International Aerospace Abstracts*, 1999 *Technical Digest*, 1992 **Electrical & Electronics Abstracts**, 1997

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