

## Sparse matrix-vector multiplication on network-on-chip

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**Abstract.** In this paper, we present an idea for performing matrix-vector multiplication by using Network-on-Chip (NoC) architecture. In traditional IC design on-chip communications have been designed with dedicated point-to-point interconnections. Therefore, regular local data transfer is the major concept of many parallel implementations. However, when dealing with the parallel implementation of sparse matrix-vector multiplication (SMVM), which is the main step of all iterative algorithms for solving systems of linear equation, the required data transfers depend on the sparsity structure of the matrix and can be extremely irregular. Using the NoC architecture makes it possible to deal with arbitrary structure of the data transfers; i.e. with the irregular structure of the sparse matrices. So far, we have already implemented the proposed SMVM-NoC architecture with the size  $4 \times 4$  and  $5 \times 5$  in IEEE 754 single float point precision using FPGA.

### 1 Introduction

Over the past 30 years, scientists have tried to mitigate the poor performance of sparse matrix computations through various approaches, such as reordering the data to reduce wasted memory bandwidth, modifying the algorithms to reuse the data, and even building specialized memory controllers. Despite these efforts, sparse matrix performance on GPPs (General Purpose Processors) still depends on the sparsity structure of the matrices (Morris and Prasanna, 2007).

Sparse matrix computations occur in various applications. For example, the Finite Element Method (FEM) is a widely used engineering analysis tool based on obtaining a numerically approximate solution for a given mathematical model of a structure. The resulting linear system is characterized

by the system matrix  $A$  which is usually large and sparse (Elkurdí et al., 2008). Iterative solvers, mainly the Conjugate Gradient (CG) method, are almost dominated by SMVM operations. The CG method is the best-known iterative method for numerically solving linear equation,  $A \cdot x = b$ , whenever  $A$  is a Symmetric Positive-Definite (SPD) sparse matrix. In the past few years, many researchers have presented the hardware solutions utilizing the feature of the pipeline ability and the parallelism inherent from the SMVM computation (Sun et al., 2007; Gregg et al., 2007; Götzte and Schwiegelshohn, 1988; Williams et al., 2007). On the other hand, Google's PageRank (PR) Eigenvalue problem is the world's largest sparse matrix calculation. This algorithm is almost dominated by SMVM operations where the target matrix is extremely sparse, unsymmetrical and unstructured. This problem has also been investigated for acceleration with a FPGA solution in (McGonrick et al., 2008; Zhuo and Prasanna, 2005).

Traditional architectures of SMVM implementations usually focused on a dedicated internal chip interconnection to forward the vector components and nonzero matrix elements between multiple processors. For example, the fat-tree style designs, which required presorting and preordering before input the data (Kapre and DeHon, 2007), will become extremely difficult when the matrix is very large and sparse. This challenge brings current applications and technology trends to motivate a paradigm shift in on-chip interconnect architectures from bus-based point-to-point network to packet-based switch network. This packet-based architecture is called Network-on-Chip (NoC) (Bertozzi and Benini, 2004; Wolf, 2004). The basic idea of the NoC is that we regard a Systems-on-Chip (SoC) device as a micro network of components. In this paper, in order to solve the problems arising from large sparse matrices with their extremely irregular structures, we select a chip-internal NoC architecture as the main transmission network base for the data transfers required for the SMVM (SMVM-NoC). Utilizing the packets forwarding functionality is beneficial concerning



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# Sparse Matrix Vector Multiplication Based Network

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## **Sparse Matrix Vector Multiplication Based Network:**

**Sparse Matrix-Vector Multiplication Based on Network-on-Chip** Ahmad Mansour,2015 Neuroscience, computing, performance, and benchmarks: Why it matters to neuroscience how fast we can compute Felix Schürmann,Omar Awile,James Courtney Knight,Thomas Nowotny,James B. Aimone,Markus Diesmann,2023-04-26 *Real-Time Electromagnetic Transient Simulation of AC-DC Networks* Venkata Dinavahi,Ning Lin,2021-06-14 Explore a comprehensive and state of the art presentation of real time electromagnetic transient simulation technology by leaders in the field Real Time Electromagnetic Transient Simulation of AC DC Networks delivers a detailed exposition of field programmable gate array FPGA hardware based real time electromagnetic transient EMT emulation for all fundamental equipment used in AC DC power grids The book focuses specifically on detailed device level models for their hardware realization in a massively parallel and deeply pipelined manner as well as decomposition techniques for emulating large systems Each chapter contains fundamental concepts apparatus models solution algorithms and hardware emulation to assist the reader in understanding the material contained within Case studies are peppered throughout the book ranging from small didactic test circuits to realistically sized large scale AC DC grids The book also provides introductions to FPGA and hardware in the loop HIL emulation procedures and large scale networks constructed by the foundational components described in earlier chapters With a strong focus on high voltage direct current power transmission grid applications Real Time Electromagnetic Transient Simulation of AC DC Networks covers both system level and device level mathematical models Readers will also enjoy the inclusion of A thorough introduction to field programmable gate array technology including the evolution of FPGAs technology trends hardware architectures and programming tools An exploration of classical power system components e g linear and nonlinear passive power system components transmission lines power transformers rotating machines and protective relays A comprehensive discussion of power semiconductor switches and converters i e AC DC and DC DC converters and specific power electronic apparatus such as DC circuit breakers An examination of decomposition techniques used at the equipment level as well as the large scale system level for real time EMT emulation of AC DC networks Chapters that are supported by simulation results from well defined test cases and the corresponding system parameters are provided in the Appendix Perfect for graduate students and professional engineers studying or working in electrical power engineering Real Time Electromagnetic Transient Simulation of AC DC Networks will also earn a place in the libraries of simulation specialists senior modeling and simulation engineers planning and design engineers and system studies engineers **Smart Infrastructure and Applications** Rashid Mehmood,Simon See,Iyad Katib,Imrich Chlamtac,2019-06-20 This book provides a multidisciplinary view of smart infrastructure through a range of diverse introductory and advanced topics The book features an array of subjects that include smart cities and infrastructure e healthcare emergency and disaster management Internet of Vehicles supply chain management eGovernance and high performance computing The book is divided into five parts

Smart Transportation Smart Healthcare Miscellaneous Applications Big Data and High Performance Computing and Internet of Things IoT Contributions are from academics researchers and industry professionals around the world Features a broad mix of topics related to smart infrastructure and smart applications particularly high performance computing big data and artificial intelligence Includes a strong emphasis on methodological aspects of infrastructure technology and application development Presents a substantial overview of research and development on key economic sectors including healthcare and transportation

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**2008 37th International Conference on Parallel Processing** IEEE Staff, 2008 **Energy Research Abstracts** ,1987 **The 1994 IEEE International Conference on Neural Networks** ,1994

Proceedings of Technical Papers ,2005 **Systolic Arrays, Papers Presented at the First INT Workshop on Systolic Arrays, Oxford 2-4 July 1986** Will Moore, Andrew McCabe, Roddy Urquhart, 1987 This book contains the edited proceedings of the First International Workshop on Systolic Arrays The workshop was the second in a series on topics in VLSI the first being on Wafer Scale Integration and brought together workers in the field of systolic arrays and related SIMD architectures from around the world The papers in this volume have been selected to cover all major aspects of systolic arrays design methodologies simulation and formal synthesis algorithms and architectures applications and chip designs testing and fault tolerance wavefront arrays and SIMD alternatives Systolic arrays along with other parallel computer designs are becoming important for many applications there is currently a large research effort being devoted to them and commercial ICs are becoming available Therefore this book is a very timely introduction to and summary of the present state of development The editors Dr Will Moore has been involved in research into VLSI architectures including systolic arrays for six years and has a special interest in regular arrays testing fault tolerance and very large circuits He initiated the First International Workshop on Wafer Scale Integration in 1985 Adam Hilger 1986 and is planning events on

Hardware Accelerators and Designing for Yield Andrew McCabe has been involved in integrated circuit design and applications for eleven years For the last six years he has managed a VLSI architectures research and development team and has worked on the design of several systolic array ICs His current interests include parallel processing systolic algorithms and architecture formal design methods fault tolerance and wafer scale integration Dr Roddy Urquhart has worked on the research and development of systolic array architectures for four years He is currently managing a development programme of high performance ICs for digital signal processing

*Introduction to Parallel Computing* Vipin Kumar, 1994 Mathematics of Computing Parallelism **FPGA ...**, 2005 **Parallel Computing on Heterogeneous Networks** Alexey Lastovetsky, 2003-06-19 New approaches to parallel computing are being developed that make better use of the heterogeneous cluster architecture Provides a detailed introduction to parallel computing on heterogeneous clusters All concepts and algorithms are illustrated with working programs that can be compiled and executed on any cluster The algorithms discussed have practical applications in a range of real life parallel computing problems such as the N body problem portfolio management and the modeling of oil extraction

*Cyberinfrastructure Technologies and Applications* Junwei Cao, 2009 Cyberinfrastructure was proposed in a report of the NSF Blue Ribbon advisory panel in 2003 Cyberinfrastructure will provide a unified environment to access and manage cyber resources e g supercomputers data archives software services scientific instruments and virtual organisations In this book the authors review latest research and development and discuss new technologies and applications involved in building Cyberinfrastructure The purpose of this book is to provide a detailed summary of early experiences practices and lessons learned in building Cyberinfrastructure from multiple perspectives software development and maintenance resource integration and sharing cyber environment construction operation and management testing and troubleshooting application enabling security and QoS ensuring Consequently this book can serve as a valuable source of reference and indispensable reading for researchers educators engineers graduate students and practitioners in the field of design and implementation of Cyberinfrastructure systems

**Toward Teraflop Computing and New Grand Challenge Applications** R. K. Kalia, 1995 *Toward Teraflop Computing New Grand Challenge Applications Proceedings of the Mardi Gras 94 Conference February 10 12 1994 Louisiana State University* **Government Reports Annual Index**, 1993 Mathematical Reviews, 2005 Journal of Information Science and Engineering, 2002 Conference Proceedings of the 1997 International Conference on Supercomputing, 1997 Proceedings Parallel Computing **Proceedings of the ACM ... Java Grande/ISCOPE Conference**, 2002

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