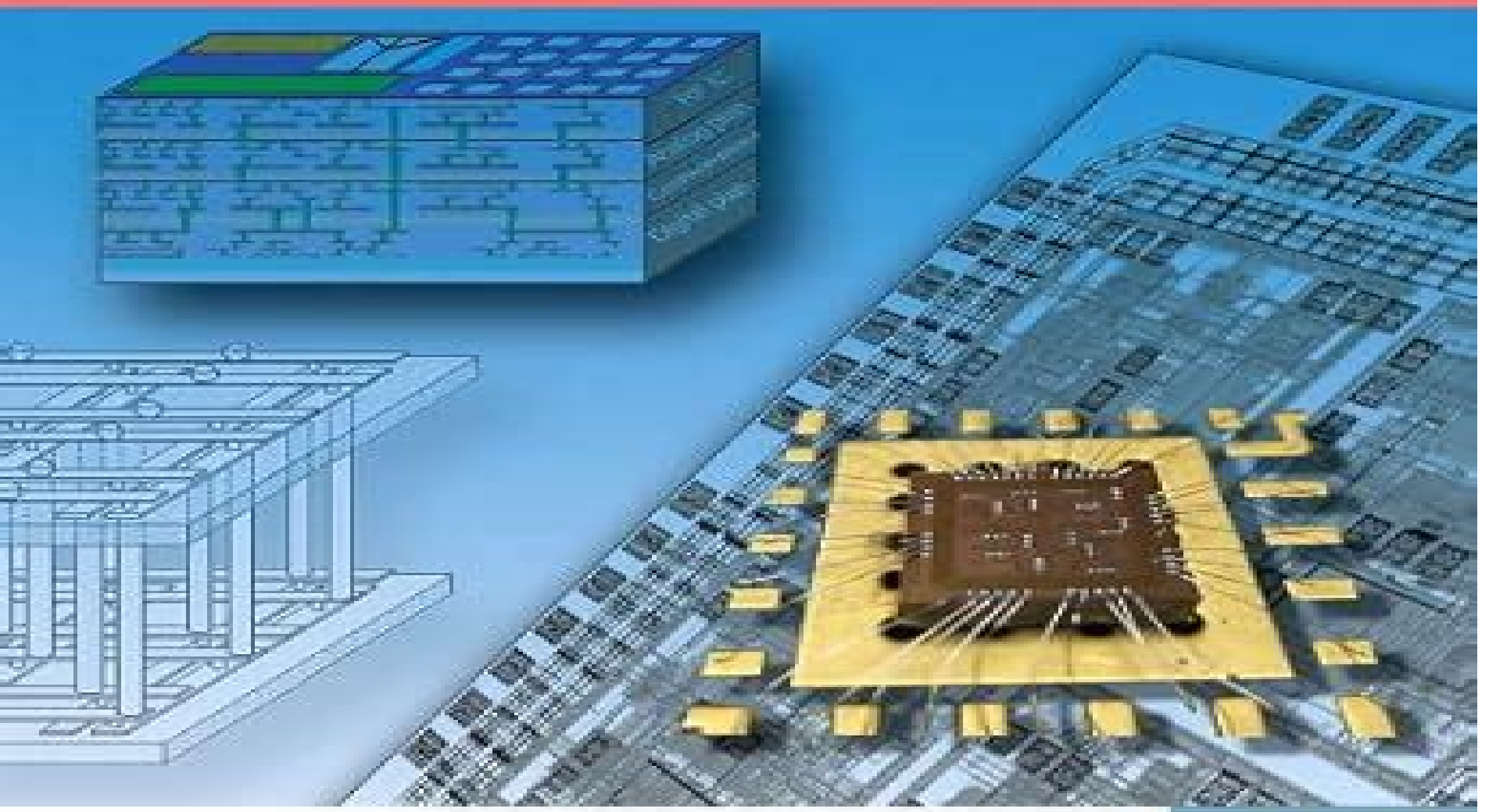

THREE-DIMENSIONAL INTEGRATED CIRCUIT DESIGN

VASILIS F. PAVLIDIS EBY G. FRIEDMAN

SYSTEMS ON SILICON

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Three Dimensional Integrated Circuit Design Systems On Silicon

Aida Todri-Sanial,Chuan Seng Tan

Three Dimensional Integrated Circuit Design Systems On Silicon:

Three-dimensional Integrated Circuit Design Vasilis F. Pavlidis,Eby G. Friedman,2010-07-28 With vastly increased complexity and functionality in the nanometer era i e hundreds of millions of transistors on one chip increasing the performance of integrated circuits has become a challenging task Connecting effectively interconnect design all of these chip elements has become the greatest determining factor in overall performance 3 D integrated circuit design may offer the best solutions in the near future This is the first book on 3 D integrated circuit design covering all of the technological and design aspects of this emerging design paradigm while proposing effective solutions to specific challenging problems concerning the design of 3 D integrated circuits A handy comprehensive reference or a practical design guide this book provides a sound foundation for the design of 3 D integrated circuits Demonstrates how to overcome interconnect bottleneck with 3 D integrated circuit design leading edge design techniques offer solutions to problems performance power consumption price faced by all circuit designers The FIRST book on 3 D integrated circuit design provides up to date information that is otherwise difficult to find Focuses on design issues key to the product development cycle good design plays a major role in exploiting the implementation flexibilities offered in the 3 D Provides broad coverage of 3 D integrated circuit design including interconnect prediction models thermal management techniques and timing optimization offers practical view of designing 3 D circuits *Three-Dimensional Integrated Circuit Design* Vasilis F. Pavlidis,Ioannis Savidis,Eby G. Friedman,2017-07-04 Three Dimensional Integrated Circuit Design Second Eition expands the original with more than twice as much new content adding the latest developments in circuit models temperature considerations power management memory issues and heterogeneous integration 3 D IC experts Pavlidis Savidis and Friedman cover the full product development cycle throughout the book emphasizing not only physical design but also algorithms and system level considerations to increase speed while conserving energy A handy comprehensive reference or a practical design guide this book provides effective solutions to specific challenging problems concerning the design of three dimensional integrated circuits Expanded with new chapters and updates throughout based on the latest research in 3 D integration Manufacturing techniques for 3 D ICs with TSVs Electrical modeling and closed form expressions of through silicon vias Substrate noise coupling in heterogeneous 3 D ICs Design of 3 D ICs with inductive links Synchronization in 3 D ICs Variation effects on 3 D ICs Correlation of WID variations for intra tier buffers and wires Offers practical guidance on designing 3 D heterogeneous systems Provides power delivery of 3 D ICs Demonstrates the use of 3 D ICs within heterogeneous systems that include a variety of materials devices processors GPU CPU integration and more Provides experimental case studies in power delivery synchronization and thermal characterization **Three-Dimensional Integrated Circuit Design** Yuan Xie,Jingsheng Jason Cong,Sachin Sapatnekar,2009-12-02 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore s law This observation stated that transistor density

in integrated circuits doubles every 1 5 2 years This came with the simultaneous improvement of individual device perf mance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore s law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device o state currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with mul ple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be ef ciently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs **Design of 3D Integrated Circuits and Systems** Rohit Sharma,2018-09-03 Three dimensional 3D integration of microsystems and subsystems has become essential to the future of semiconductor technology development 3D integration requires a greater understanding of several interconnected systems stacked over each other While this vertical growth profoundly increases the system functionality it also exponentially increases the design complexity Design of 3D Integrated Circuits and Systems tackles all aspects of 3D integration including 3D circuit and system design new processes and simulation techniques alternative communication schemes for 3D circuits and systems application of novel materials for 3D systems and the thermal challenges to restrict power dissipation and improve performance of 3D systems Containing contributions from experts in industry as well as academia this authoritative text Illustrates different 3D integration approaches such as die to die die to wafer and wafer to wafer Discusses the use of interposer technology and the role of Through Silicon Vias TSVs Presents the latest improvements in three major fields of thermal management for multiprocessor systems on chip MPSoCs Explores ThruChip Interface TCI NAND flash memory stacking and emerging applications Describes large scale integration testing and state of the art low power testing solutions Complete with experimental results of chip level 3D integration schemes tested at IBM and case studies on advanced complementary metal oxide semiconductor CMOS integration for 3D integrated circuits ICs Design of 3D Integrated Circuits and Systems is a practical reference that not only covers a wealth of design issues encountered in 3D integration but also demonstrates their impact on the efficiency of 3D systems *Physical Design for 3D Integrated Circuits* Aida Todri-Sanial,Chuan Seng Tan,2017-12-19 Physical Design for 3D Integrated Circuits reveals how to effectively and optimally design 3D integrated circuits ICs It also analyzes the design tools for 3D circuits while exploiting the benefits of 3D technology The book begins by offering an overview of physical design challenges with respect to conventional 2D circuits and then each chapter delivers an in depth look at a specific physical design topic This comprehensive reference Contains

extensive coverage of the physical design of 2 5D 3D ICs and monolithic 3D ICs Supplies state of the art solutions for challenges unique to 3D circuit design Features contributions from renowned experts in their respective fields Physical Design for 3D Integrated Circuits provides a single convenient source of cutting edge information for those pursuing 2 5D 3D technology **Arbitrary Modeling of TSVs for 3D Integrated Circuits** Khaled Salah,Yehea Ismail,Alaa El-Rouby,2014-08-21 This book presents a wide band and technology independent SPICE compatible RLC model for through silicon vias TSVs in 3D integrated circuits This model accounts for a variety of effects including skin effect depletion capacitance and nearby contact effects Readers will benefit from in depth coverage of concepts and technology such as 3D integration Macro modeling dimensional analysis and compact modeling as well as closed form equations for the through silicon via parasitics Concepts covered are demonstrated by using TSVs in applications such as a spiral inductor and inductive based communication system and bandpass filtering *3D Integration in VLSI Circuits* Katsuyuki Sakuma,2018-04-17 Currently the term 3D integration includes a wide variety of different integration methods such as 2 5 dimensional 2 5D interposer based integration 3D integrated circuits 3D ICs 3D systems in package SiP 3D heterogeneous integration and monolithic 3D ICs The goal of this book is to provide readers with an understanding of the latest challenges and issues in 3D integration TSVs are not the only technology element needed for 3D integration There are numerous other key enabling technologies required for 3D integration and the speed of the development in this emerging field is very rapid To provide readers with state of the art information on 3D integration research and technology developments each chapter has been contributed by some of the world s leading scientists and experts from academia research institutes and industry from around the globe Covers chip wafer level 3D integration technology memory stacking reconfigurable 3D and monolithic 3D IC Discusses the use of silicon interposer and organic interposer Presents architecture design and technology implementations for 3D FPGA integration Describes oxide bonding Cu SiO2 hybrid bonding adhesive bonding and solder bonding Addresses the issue of thermal dissipation in 3D integration *High Performance Integrated Circuit Design* Emre Salman,Eby G. Friedman,2012-08-14 The latest techniques for designing robust high performance integrated circuits in nanoscale technologies Focusing on a new technological paradigm this practical guide describes the interconnect centric design methodologies that are now the major focus of nanoscale integrated circuits ICs High Performance Integrated Circuit Design begins by discussing the dominant role of on chip interconnects and provides an overview of technology scaling The book goes on to cover data signaling power management synchronization and substrate aware design Specific design constraints and methodologies unique to each type of interconnect are addressed This comprehensive volume also explains the design of specialized circuits such as tapered buffers and repeaters for data signaling voltage regulators for power management and phase locked loops for synchronization This is an invaluable resource for students researchers and engineers working in the area of high performance ICs Coverage includes Technology scaling Interconnect modeling and

extraction Signal propagation and delay analysis Interconnect coupling noise Global signaling Power generation Power distribution networks CAD of power networks Techniques to reduce power supply noise Power dissipation Synchronization theory and tradeoffs Synchronous system characteristics On chip clock generation and distribution Substrate noise in mixed signal ICs Techniques to reduce substrate noise **W-band Three-dimensional Integrated Circuits Utilizing Silicon Micromachining** Katherine Juliet Herrick,2000 **Three Dimensional System Integration** Antonis Papanikolaou,Dimitrios Soudris,Riko Radojcic,2010-12-07 Three dimensional 3D integrated circuit IC stacking is the next big step in electronic system integration It enables packing more functionality as well as integration of heterogeneous materials devices and signals in the same space volume This results in consumer electronics e g mobile handheld devices which can run more powerful applications such as full length movies and 3D games with longer battery life This technology is so promising that it is expected to be a mainstream technology a few years from now less than 10 15 years from its original conception To achieve this type of end product changes in the entire manufacturing and design process of electronic systems are taking place This book provides readers with an accessible tutorial on a broad range of topics essential to the non expert in 3D System Integration It is an invaluable resource for anybody in need of an overview of the 3D manufacturing and design chain **System Design of Multi-Layer (Three Dimensional) Integrated Circuits** J. F. Gibbons,STANFORD UNIV CA STANFORD ELECTRONICS LABS.,1985 Research carried out on beam processing of semiconductors led to the concept of a three dimensional integrated circuit It was shown that MOS devices could be made on both sides of a laser recrystallized thin film of silicon deposited on an insulating substrate SOI and also on vertically arranged recrystallized silicon films separated by insulating layers of silicon dioxide and or silicon nitride oxide combinations It follows from these observations that integrated circuits can be made by vertically interconnecting devices made on separate layers Such circuits could lead to improved packing density which would be important for memory applications and possibly to increased circuit speed which would be important for logic application 3D Integration for VLSI Systems Chuan Seng Tan,Kuan-Neng Chen,Steven J. Koester,2011-09-26 Three dimensional 3D integration is identified as a possible avenue for continuous performance growth in integrated circuits IC as the conventional scaling approach is faced with unprecedented challenges in fundamental and economic limits Wafer level 3D IC can take several forms and they usually include a stack of several thinned IC layers that are vertically bonded and interconnected by through silicon via TSV There is a long string of benefits that one can derive from 3D IC implementation such as form factor density multiplication improved delay and power enhanced bandwidth and heterogeneous integration This book presents contributions by key researchers in this field covering motivations technology platforms applications and other design issues *2005 International Conference on Integrated Circuit Design and Technology* ,2005 Issues for 2009 cataloged as a serial in LC Circuits and Systems for Three-dimensional Integration Technology Christianto Chih-Ching Liu,2006 **Electrical Design of Through Silicon Via** Manho Lee,Jun So Pak,Joungho

Kim,2014-05-11 Through Silicon Via TSV is a key technology for realizing three dimensional integrated circuits 3D ICs for future high performance and low power systems with small form factors This book covers both qualitative and quantitative approaches to give insights of modeling TSV in a various viewpoints such as signal integrity power integrity and thermal integrity Most of the analysis in this book includes simulations numerical modelings and measurements for verification The author and co authors in each chapter have studied deep into TSV for many years and the accumulated technical know hows and tips for related subjects are comprehensively covered **Electrical Modeling and Design for 3D System Integration** Er-Ping Li,2012-04-10 New advanced modeling methods for simulating the electromagnetic properties of complex three dimensional electronic systems Based on the author s extensive research this book sets forth tested and proven electromagnetic modeling and simulation methods for analyzing signal and power integrity as well as electromagnetic interference in large complex electronic interconnects multilayered package structures integrated circuits and printed circuit boards Readers will discover the state of the technology in electronic package integration and printed circuit board simulation and modeling In addition to popular full wave electromagnetic computational methods the book presents new more sophisticated modeling methods offering readers the most advanced tools for analyzing and designing large complex electronic structures Electrical Modeling and Design for 3D System Integration begins with a comprehensive review of current modeling and simulation methods for signal integrity power integrity and electromagnetic compatibility Next the book guides readers through The macromodeling technique used in the electrical and electromagnetic modeling and simulation of complex interconnects in three dimensional integrated systems The semi analytical scattering matrix method based on the N body scattering theory for modeling of three dimensional electronic package and multilayered printed circuit boards with multiple vias Two and three dimensional integral equation methods for the analysis of power distribution networks in three dimensional package integrations The physics based algorithm for extracting the equivalent circuit of a complex power distribution network in three dimensional integrated systems and printed circuit boards An equivalent circuit model of through silicon vias Metal oxide semiconductor capacitance effects of through silicon vias Engineers researchers and students can turn to this book for the latest techniques and methods for the electrical modeling and design of electronic packaging three dimensional electronic integration integrated circuits and printed circuit boards **Materials and Technologies for 3-D Integration** Fred Roozeboom,2009 **3D IC Integration and Packaging** John H. Lau,2015-07-06 A comprehensive guide to 3D IC integration and packaging technology3D IC Integration and Packaging fully explains the latest microelectronics techniques for increasing chip density and maximizing performance while reducing power consumption Based on a course developed by its author this practical guide offers real world problem solving methods and teaches the trade offs inherent in making system level decisions Explore key enabling technologies such as TSV thin wafer strength measurement and handling microsolder bumping redistribution layers interposers wafer to wafer bonding chip to

wafer bonding 3D IC and MEMS LED and complementary metal oxide semiconductor image sensors integration Assembly thermal management and reliability are covered in complete detail 3D IC Integration and Packaging covers 3D integration for semiconductor IC packaging Through silicon vias modeling and testing Stress sensors for thin wafer handling and strength measurement Package substrate technologies Microbump fabrication assembly and reliability 3D Si integration 2 5D 3D IC integration 3D IC integration with passive interposer Thermal management of 2 5D 3D IC integration Embedded 3D hybrid integration 3D LED and IC integration 3D MEMS and IC integration 3D CMOS image sensors and IC integration PoP chip to chip interconnects and embedded fan out WLP Three Dimensional Integrated Circuit Design and Test Jing Xie,2015 The emerging three dimensional integrated circuits 3D ICs is one of the most promising solutions for future IC designs 3D stacking enables much higher memory bandwidth and much lower overhead in multi power domain design which provides solutions for chip multiprocessor design in mitigating the memory wall and dark silicon problem At the same time 3D technology leads to new opportunities and challenges in the field of circuit and system design techniques EDA tools and chip testing mechanism This dissertation presents two killer applications for the modern 3D system and one 3D testing solution The first contribution of this dissertation is to propose a killer application for TSV based system the 3D memory stacking This dissertation presents a 3D memory stacking system that leverages the massive number of TSVs between memory layers to help high bandwidth checkpointing restore To validate the proposed scheme 2 layer TSV based SRAM SRAM 3D stacked chip is implemented to mimic the high bandwidth and fast data transfer from one memory layer to another memory layer so that the in memory checkpointing restore scheme can be enabled for the future exascale computing The capacity of each SRAM layer is 1 Mbit Each layer contains 64 banks with each bank contains 256 words and the word length is 64 bit The final footprint including I O pad is 2 9mm X 2mm The SRAM dies were taped out in GlobalFoundries using its 130nm low power process and the 3D stacking was done by using Tezzaron s TSV technology The prototyping chip can perform checkpointing restore at the speed of 4K cycle with 1Ghz clock This dissertation also gives an applicable solution for 3D testing Testing for 3D ICs based on through silicon via TSV is one of the major challenges for improving the system yield and reducing the overall cost The lack of pads on most tiers and the mechanical vulnerability of tiers after wafer thinning make it difficult to perform 3D Known Good Die KGD test with the existing 2D IC probing methods This dissertation presents a novel and time efficient 3D testing flow In this Known Good Stack KGS flow a yield aware TSV defect searching and replacing strategy is introduced The Build in Self Test BIST design with TSV redundancy scheme help improve the system yield for today s imperfect TSV fabrication process Our study shows that less than 6 redundant TSVs is enough to increase the TSV yield to 98% for a TSV cluster with a size under 16 X 16 with relatively low initial TSV yield The average TSV cluster testing and self fixing time is about 3 16 testing cycle depending on the initial TSV yield The second killer application for 3D system in this dissertation is multi power domain system design utilizing the monolithic technology Optimizing energy

consumption for electronic systems has been an important design consideration Among all the techniques multi power domain design is a widely used one for low power and high performance applications In order to perform the data transfer between these different power domains we needs a cross power domain interface CPDI The existing level conversion flip flop LCFF structures all require dual power rails which results in large area and performance overhead We proposed a scan able CPDI circuit utilizing monolithic 3D technology This interface functions as a flip flop and provides reliable data conversion from one power domain to another It also has built in scan feature which makes it testable Our design separates power rails in each tier substantially reduced physical design complexity and area penalty The design is implemented in a 20nm 28nm and 45nm low power technology It shows 20% 35% smaller D to Q comparing with normal designs The proposed design also shows scalability and better energy consumption than precious LCFF design Finally we presented a dual power domain deep pipeline circuit architecture for future power efficient systems We reduce the power consumption by putting all the combinational logics in a lower power domain while all the FFs and clock network operate at normal voltage for smaller insertion delay and better clock control In order to realize these functions and system benefits we proposed a novel level conversion flip flop omega design which has 30% insertion delay than the normal flop design and could be easily integrated into today s synthesis flow This work provides guideline on how to design a dual power domain system with less power under the same system throughput requirement A system level estimation shows that the 3D dual power supply system could consume about 15% less energy by using our design methodology *International Symposium on Quality Electronic Design* ,2002 Annotation Fifty one papers and 21 posters from the March 2002 symposium report current research in deep submicron integrated circuit design and development The sessions address interconnect extraction and modeling design for process variations metrics power and noise management verification signal integrity and low power design techniques Some of the topics are transition aware global signaling TAGS the interoperability of EDA tools for sequential logic synthesis statistical methods for the determination of process corners power supply noise suppression via clock skew scheduling and the relation between SAT and BDDs for equivalence checking No subject index Annotation copyrighted by Book News Inc Portland OR

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