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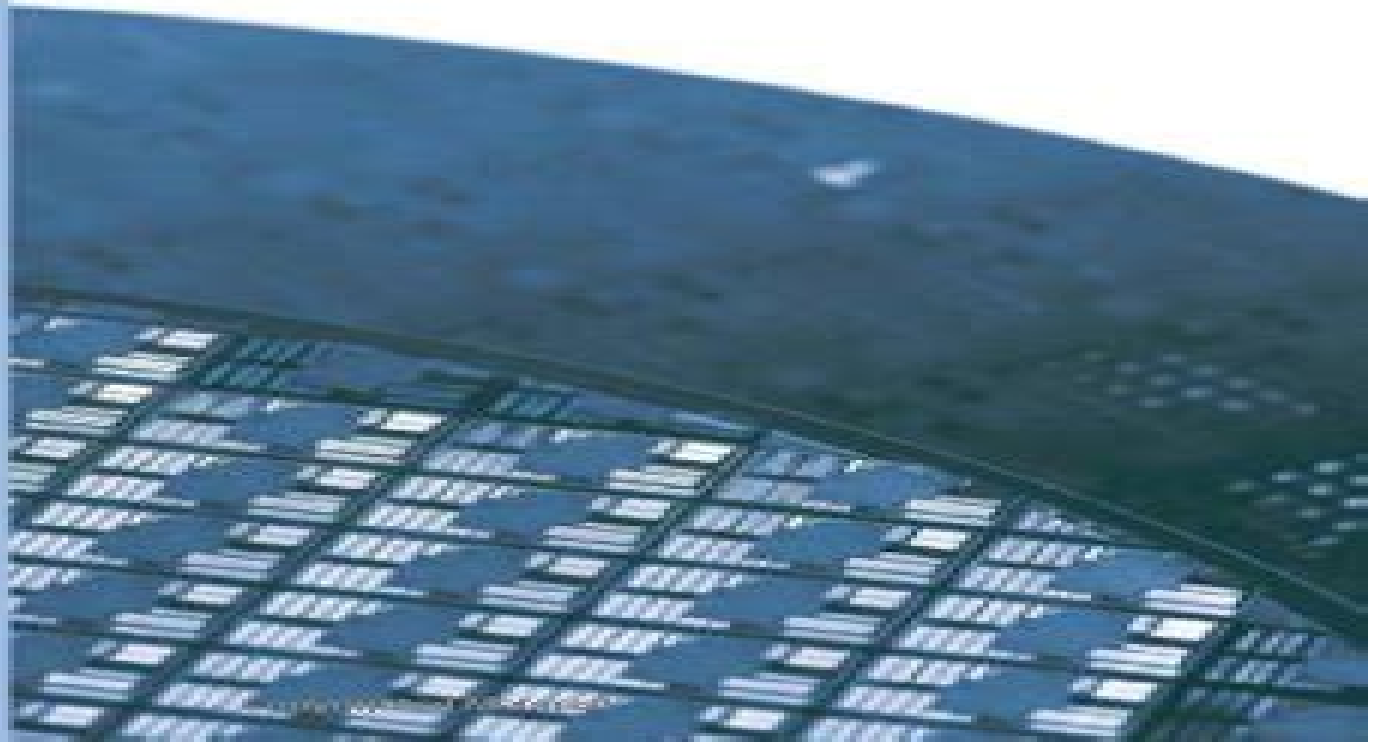
Wafer-Level Testing and Test During Burn-In for Integrated Circuits

Sudarshan Bahukudumbi
Krishnendu Chakrabarty



Wafer Level Testing And Test During Burn In For Integrated Circuits Integrated Mircosystems

Yehya H. Ghallab,Wael Badawy

Wafer Level Testing And Test During Burn In For Integrated Circuits Integrated Mircosystems:

Wafer-level Testing and Test During Burn-in for Integrated Circuits Sudarshan Bahukudumbi,Krishnendu Chakrabarty,2010 Wafer level testing refers to a critical process of subjecting integrated circuits and semiconductor devices to electrical testing while they are still in wafer form Burn in is a temperature bias reliability stress test used in detecting and screening out potential early life device failures This hands on resource provides a comprehensive analysis of these methods showing how wafer level testing during burn in WLTBI helps lower product cost in semiconductor manufacturing Engineers learn how to implement the testing of integrated circuits at the wafer level under various resource constraints Moreover this unique book helps practitioners address the issue of enabling next generation products with previous generation testers Practitioners also find expert insights on current industry trends in WLTBI test solutions **Lab-on-a-chip** Yehya H. Ghallab,Wael Badawy,2010 HereOCOs a groundbreaking book that introduces and discusses the important aspects of lab on a chip including the practical techniques circuits microsystems and key applications in the biomedical biology and life science fields Moreover this volume covers ongoing research in lab on a chip integration and electric field imaging Presented in a clear and logical manner the book provides you with the fundamental underpinnings of lab on a chip presents practical results and brings you up to date with state of the art research in the field This unique resource is supported with over 160 illustrations that clarify important topics throughout *Microelectronics Fialure Analysis Desk Reference, Seventh Edition* Tejinder Gandhi,2019-11-01 The Electronic Device Failure Analysis Society proudly announces the Seventh Edition of the Microelectronics Failure Analysis Desk Reference published by ASM International The new edition will help engineers improve their ability to verify isolate uncover and identify the root cause of failures Prepared by a team of experts this updated reference offers the latest information on advanced failure analysis tools and techniques illustrated with numerous real life examples This book is geared to practicing engineers and for studies in the major area of power plant engineering For non metallurgists a chapter has been devoted to the basics of material science metallurgy of steels heat treatment and structure property correlation A chapter on materials for boiler tubes covers composition and application of different grades of steels and high temperature alloys currently in use as boiler tubes and future materials to be used in supercritical ultra supercritical and advanced ultra supercritical thermal power plants A comprehensive discussion on different mechanisms of boiler tube failure is the heart of the book Additional chapters detailing the role of advanced material characterization techniques in failure investigation and the role of water chemistry in tube failures are key contributions to the book

Highly Integrated Microfluidics Design Dan E. Angelescu,2011 The recent development of microfluidics has lead to the concept of lab on a chip where several functional blocks are combined into a single device that can perform complex manipulations and characterizations on the microscopic fluid sample However integration of multiple functionalities on a single device can be complicated This a cutting edge resource focuses on the crucial aspects of integration in microfluidic

systems It serves as a one stop guide to designing microfluidic systems that are highly integrated and scalable This practical book covers a wide range of critical topics from fabrication techniques and simulation tools to actuation and sensing functional blocks and their inter compatibility This unique reference outlines the benefits and drawbacks of different approaches to microfluidic integration and provides a number of clear examples of highly integrated microfluidic systems

RFID-enabled Sensor Design and Applications Amin Rida,Li Yang,Manos M. Tentzeris,2010 RFID radio frequency identification is an emerging communication system technology and one of the most rapidly growing segments of todayOCOs automatic identification data collection industry This cutting edge resource offers you a solid understanding of the basic technical principles and applications of RFID enabled sensor systems The book provides you with a detailed description of RFID and itOCOs operation along with a fundamental overview of sensors and wireless sensor networks Moreover this practical reference gives you step by step guidance on how to design RFID enabled sensors that form a wireless sensor network You also find detailed coverage of state of OCothe art RFID sensor technology and worldwide applications

Microfabrication for Microfluidics Sang-Joon John Lee,Narayanan Sundararajan,2010 Providing a definitive source of knowledge about the principles materials and process techniques used in the fabrication of microfluidics this practical volume is a must for your reference shelf The book focuses on fabrication but also covers the basic purpose benefits and limitations of the fabricated structures as they are applied to microfluidic sensor and actuator functions You find guidance on rapidly assessing options and tradeoffs for the selection of a fabrication method with clear tabulated process comparisons

Acoustic Wave and Electromechanical Resonators Humberto Campanella,2010 This groundbreaking book provides you with a comprehensive understanding of FBAR thin film bulk acoustic wave resonator MEMS microelectomechanical system and NEMS nanoelectromechanical system resonators For the first time anywhere you find extensive coverage of these devices at both the technology and application levels This practical reference offers you guidance in design fabrication and characterization of FBARs MEMS and NEBS It discusses the integration of these devices with standard CMOS complementary metal oxide semiconductor technologies and their application to sensing and RF systems Moreover this one stop resource looks at the main characteristics differences and limitations of FBAR MEMS and NEMS devices helping you to choose the right approaches for your projects Over 280 illustrations and more than 130 equations support key topics throughout the book **Design of Systems on a Chip: Design and Test** Ricardo Reis,Marcelo Soares Lubaszewski,Jochen A.G. Jess,2007-05-06 This book is the second of two volumes addressing the design challenges associated with new generations of semiconductor technology The various chapters are compiled from tutorials presented at workshops in recent years by prominent authors from all over the world Technology productivity and quality are the main aspects under consideration to establish the major requirements for the design and test of upcoming systems on a chip *Wafer-Level Testing and Test Planning for Integrated Circuits* Sudarshan Bahukudumbi,2008 The relentless scaling of semiconductor

devices and high integration levels have lead to a steady increase in the cost of manufacturing test for integrated circuits ICs The higher test cost leads to an increase in the product cost of ICs Product cost is a major driver in the consumer electronics market which is characterized by low profit margins and the use of a variety of core based system on chip SoC designs Packaging has also been recognized as a significant contributor to the product cost for SoCs Packaging cost and the test cost for packaged chips can be reduced significantly by the use of effective test methods at the wafer level also referred to as wafer sort Test application time is a major practical constraint for wafer sort even more than for package test Therefore not all the scan based digital test patterns can be applied to the die under test This thesis first presents a test length selection technique for wafer level testing of core based SoCs This optimization technique which is based on a combination of statistical yield modeling and integer linear programming ILP provides the pattern count for each embedded core during wafer sort such that the probability of screening defective dies is maximized for a given upper limit on the SoC test time A large number of wafer probe contacts can potentially lead to higher yield loss during wafer sort An optimization framework is therefore presented to address test access mechanism TAM optimization and test length selection for wafer level testing when constraints are placed on the number of number of chip pins that can be contacted Next a correlation based signature analysis technique is presented for mixed signal test at the wafer level using low cost digital testers The proposed method overcomes the limitations of measurement inaccuracies at the wafer level A generic cost model is developed to evaluate the effectiveness of wafer level testing of analog and digital cores in a mixed signal SoC and to study its impact on test escapes yield loss and packaging cost Results are presented for a typical mixed signal big D small A SoC from industry which contains a large section of flattened digital logic and several large mixed signal cores Wafer level test during burn in WLTBI is an emerging practice in the semiconductor industry that allows testing to be performed simultaneously with burn in at the wafer level However the testing of multiple cores of a SoC in parallel during WLTBI leads to constantly varying device power during the duration of the test This power variation adversely affects predictions of temperature and the time required for burn in A test scheduling technique is presented for WLTBI of core based SoCs where the primary objective is to minimize the variation in power consumption during test A secondary objective is to minimize the test application time Finally this thesis presents a test pattern ordering technique for WLTBI The objective here is to minimize the variation in power consumption during test application The test pattern ordering problem for WLTBI is solved using ILP and efficient heuristic techniques The thesis also demonstrates how test pattern manipulation and pattern ordering can be combined for WLTBI Test pattern manipulation is carried out by carefully filling the don t care X bits in test cubes The X fill problem is formulated and solved using an efficient polynomial time algorithm In summary this research is targeted at cost efficient wafer level test and burn in of current and next generation semiconductor devices The proposed techniques are expected to bridge the gap between wafer sort and package test by providing cost effective wafer scale test solutions The results of this research will

lead to higher shipped product quality lower product cost and pave the way for known good die KGD devices especially for emerging technologies such as three dimensional integrated circuits **Scientific and Technical Aerospace Reports** ,1971 System-on-Chip Test Architectures Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students *Electrical & Electronics Abstracts* ,1997 Wafer-Level Testing and Test Planning for Integrated Circuits ,2005 The relentless scaling of semiconductor devices and high integration levels have lead to a steady increase in the cost of manufacturing test for integrated circuits ICs The higher test cost leads to an increase in the product cost of ICs Product cost is a major driver in the consumer electronics market which is characterized by low profit margins and the use of a variety of core based system on chip SoC designs Packaging has also been recognized as a significant contributor to the product cost for SoCs Packaging cost and the test cost for packaged chips can be reduced significantly by the use of effective test methods at the wafer level also referred to as wafer sort Test application time is a major practical constraint for wafer sort even more than for package test Therefore not all the scan based digital test patterns can be applied to the die under test This thesis first presents a test length selection technique for wafer level testing of core based SoCs This optimization technique which is based on a combination of statistical yield modeling and integer linear programming ILP provides the pattern count for each embedded core during wafer sort such that the probability of screening defective dies is maximized for a given upper limit on the SoC test time A large number of wafer probe contacts can potentially lead to higher yield loss during wafer sort An optimization framework is therefore presented to address test access mechanism TAM optimization and test length selection for wafer level testing when constraints are placed on the number of number of chip

pins that can be contacted Next a correlation based signature analysis technique is presented for mixed signal test at the wafer level using low cost digital testers The proposed method overcomes the limitations of measurement inaccuracies at the wafer level A generic cost model is developed to evaluate the effectiveness of wafer level testing of analog and digital **A Manual Wafer Probe Station for an Integrated Circuit Test System** G. P. Carver,1981 **Wafer-Level Integrated Systems** Stuart K. Tewksbury,2012-12-06 From the perspective of complex systems conventional Ie s can be regarded as discrete devices interconnected according to system design objectives imposed at the circuit board level and higher levels in the system implementation hierarchy However silicon monolithic circuits have progressed to such complex functions that a transition from a philosophy of integrated circuits Ie s to one of integrated sys tems is necessary Wafer scale integration has played an important role over the past few years in highlighting the system level issues which will most significantly impact the implementation of complex monolithic systems and system components Rather than being a revolutionary approach wafer scale integration will evolve naturally from VLSI as defect avoidance fault tolerance and testing are introduced into VLSI circuits Successful introduction of defect avoidance for example relaxes limits imposed by yield and cost on Ie dimensions allowing the monolithic circuit s area to be chosen according to the natural partitioning of a system into individual functions rather than imposing area limits due to defect densities The term wafer level is perhaps more appropriate than wafer scale A wafer level monolithic system component may have dimensions ranging from conventional yield limited Ie dimensions to full wafer dimensions In this sense wafer scale merely represents the obvious upper practical limit imposed by wafer sizes on the area of monolithic circuits The transition to monolithic wafer level integrated systems will require a mapping of the full range of system design issues onto the design of monolithic circuit **Using IEEE 1500 for Wafer Testing of TSV Based 3D Integrated Circuits** Ryan A. Ugland,2011 The potential end of Moore s law has caused the semiconductor industry to investigate 3D integrated circuits as a way to continue to increase transistor density Solutions must be put in place to allow each 3D IC die layer to be tested thoroughly on its own at wafer level to unsure adequate yield on assembled 3D devices This paper details the testability of a 3D implementation of the Open Cores or1200 architecture IEEE 1500 is used to signi cantly improve wafer level testability of the 3D IC die layers while maintaining a low test pin count requirement Evaluation of the Wafer-level Voltage Ramp Test for Oxide Integrity Steven Drager,Rome Laboratory (Griffiss Air Force Base, N.Y.),1996 Failure Analysis of Integrated Circuits Lawrence C. Wagner,1999-01-31 This must have reference work for semiconductor professionals and researchers provides a basic understanding of how the most commonly used tools and techniques in silicon based semiconductors are applied to understanding the root cause of electrical failures in integrated circuits **High Temperature Reverse Bias Testing and Failure Mechanism Analysis of Integrated Circuits** Edgar A Doyle (Jr),Vincent C. Kapfer,ROME AIR DEVELOPMENT CENTER GRIFFISS AFB NY.,1967 Test analysis indicated that for these circuits the stress levels of the standard burn in screen test were inadequate for the

effective screening of potential circuit failures The accelerated HTRB test generated surface inversion failures at both stress temperatures where the time required for circuit degradation decreased with increasing temperature The majority of the stressed circuits exhibited excellent discrete junction reverse current stability Based upon these tests it is concluded that increasing test temperatures will be required to effectively screen out potential reverse current failures in integrated circuits using the relatively cleaner oxides available to present technology The limited availability and high cost of high temperature integrated circuit test boards may force the manufacturer to conduct high temperature burn in screen tests on a sampling basis as an alternate approach to insure high rel circuits However the validity of this type of approach to oxide integrity screen testing of high rel circuits is doubtful Accelerated Wafer-level Integrated Circuit Reliability Testing for Electromigration in Metal Interconnects with Enhanced Thermal Modeling, Structure Design, Control of Stress, and Experimental Measurements Chih-Ching Shih,1994

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